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Long-Wavelength Vertical Cavity Lasers with Air/Semiconductor Mirrors: Nanoscale Gate Technology For Silicon Mosfets

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13. ABSTRACT *(Maximum 200 Words)*

We have investigated methods to improve sub-100nm MOSFET performance. We discovered that Poly-SiGe has very attractive qualities when used as the transistor gate material. Poly-SiGe offers less boron penetration, less poly depletion, and higher hole mobility. Dynamic Threshold MOSFET (DTMOS) techniques were also investigated to allow for improved inverter drive current over a broader range of supply voltages. We applied these techniques to various passgate logic families to show how DTMOS designs can avoid speed degradation at low supply voltages.

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FINAL TECHNICAL REPORT

97-AASERT:	"Nanoscale Gate Technology for Silicon MOSFETs"
Principal Investigator:	Professor Jeffrey Bokor
Institution:	University of California, Berkeley Electronics Research Laboratory Berkeley, CA 94720
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OBJECTIVE:

To develop advanced gate technology for sub-100 nm CMOS devices which will improve drive current without compromising off-state leakage current for short-channel devices.

GATE MATERIAL FINDINGS:

Poly-SiGe is a promising gate material because dopants are more readily activated in poly-SiGE as compared to poly-Si, so that higher active dopant concentration at the gate/gate-oxide interface can be achieved in order to reduce the gate depletion effect (GDE). Detailed characterizations of poly-SiGe-gated MOSFET performance and reliability were performed in the reporting period. In addition, MOS capacitors using molybdenum (Mo) were fabricated and characterized.

Poly-$Si_{0.8}Ge_{0.2}$-gated CMOS transistors with thin (2.9nm-thick) gate oxides and gate lengths down to 100 nm were successfully fabricated. A Ge content of 20% provides the best tradeoff between reduced GDE and work-function reduction. Additionally, gate-oxide reliability was found to be improved for poly-$Si_{0.8}Ge_{0.2}$-gated as compared with poly-Si-gated devices due to reduced boron penetration. These transistors exhibit negligible GDE as well as excellent short-channel performance (small reduction in threshold voltage as gate length decreases). As a result, higher drive currents were attained with poly-$Si_{0.8}Ge_{0.2}$-gated transistors as compared with poly-Si-gated transistors. For the p-channel transistors in particular, the use of poly-$Si_{0.8}Ge_{0.2}$ resulted in 20% higher drive current. This is attributed to the higher hole mobility in poly-$Si_{0.8}Ge_{0.2}$-gated PMOS devices, due to the lower vertical electric field in the channel region. The hot-carrier reliability of poly-$Si_{0.8}Ge_{0.2}$-gated n-channel transistors was found to be comparable to that for poly-Si gated devices.

Mo-gated MOS capacitors were fabricated and their capacitance-vs.-voltage characteristics were studied. It was found that the work function of Mo shifts from a value close to that of n+ poly-Si to a value close to that of p+ poly-Si upon any high-temperature (>400C) annealing. From a comparison of the C-V characteristics before and after annealing, Mo was found to be very stable on SiO_2, and is therefore a promising metal gate-electrode material for PMOS transistors.

GATE CONNECTIVITY FINDINGS:

Coupling the gate and the body terminals of a transistor creates a Dynamic Threshold MOS transistor (DTMOS). The advantage of this coupling is to allow for greater drive current while maintaining low leakage current in low voltage circuits. During the reporting period, we have studied new DTMOS logic styles to allow for a larger range of supply voltages, demonstrated the advantage of DTMOS in various passgate logic families, and developed a trench process to allow for DTMOS implementation in bulk silicon wafers.

Traditional DTMOS gate-to-body connectivity limits the supply voltage to less than 0.6V. We have demonstrated two other techniques for inverter connectivity with a dynamic threshold that provides a significant speed enhancement over traditional CMOS

logic while allowing for an arbitrary supply voltage. We have developed similar circuit techniques using auxiliary transistors to demonstrate the performance gain in using dynamic threshold devices in various passgate logic families. These DTMOS circuit configurations avoid the typical speed degradation found in passgate logic when the supply voltage is reduced below 1V.

Because DTMOS devices require each transistor to have its own isolated body, fabricating DTMOS is much easier using Silicon on Insulator (SOI) wafers. In an effort to extend the application of DTMOS devices, we have developed a trench process to allow for body isolation in bulk silicon wafers. This will allow us to fabricate DTMOS circuits in a process scheme similar to what the majority of the semiconductor industry uses.

PERSONNEL SUPPORTED:

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Wen-Chin Lee (associated Graduate Student)
Hideki Takeuchi (associated Visiting Industrial Fellow)
Tsu-Jae King (associated Faculty)
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PUBLICATIONS:

1. T.-J. King, "Advanced gate technology for sub-0.25 micron CMOSFETs," presented at the *SPIE 1998 Symposium on Microelectronic Manufacturing* (Santa Clara, California, USA), September 1998.
2. W.-C. Lee, T.-J. King and C. Hu, "Observation of reduced boron penetration and poly-gate depletion for poly-$Si_{0.8}Ge_{0.2}$-gated PMOS devices," *IEEE Electron Device Letters*, Vol. 20, No. 1, pp.9-11, 1999.
3. W.-C. Lee, B. Watson, T.-J. King, and C. Hu, "Enhancement of PMOS device performance with poly-SiGe Gate," *IEEE Electron Device Letters*, Vol. 20, No. 5, pp. 232-234, 1999.
4. W.-C. Lee, T.-J. King and C. Hu, "Evidence of direct hole tunneling through ultrathin gate oxide using P+ poly-SiGe gate," *IEEE Electron Device Letters*, Vol. 20, No. 6, pp. 268-270, 1999.
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6. H. Takeuchi and T.-J. King, "Poly-$Si_{1-x}Ge_x$ process integration for low sheet resistance gate CMOS technology," presented at the *195th Meeting of the Electrochemical Society* (Seattle, Washington, USA), June 1999.